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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/605,293
Filing Date	June 28, 2000
First Named Inventor	David L. Chapek
Examiner Name	N.D. Richards
Art Unit	2815
Attorney Docket No.	MIO 0037 VA/40509.118/96-0831.01

METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) -0-

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X =
Independent Claims		- 3** =		X =
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

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**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY				(Complete *(if applicable)*)	
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Signature				*Date*	June 1, 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicants	: David L. Chapek
Serial No.	: 09/605,293
Filed	: June 28, 2000
Title	: SEMICONDUCTOR DEVICES INCLUDING A LAYER OF POLYCRYSTALLINE SILICON HAVING A SMOOTH MORPHOLOGY
Docket No.	: MIO 0037 VA (96-0831.01)
Examiner	: N.D. Richards
Art Unit	: 2815

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Attorney Reg. No. 29,001

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

BRIEF ON APPEAL

This is an appeal from the Office Action mailed March 3, 2004, finally rejecting claims 9-12 and 14 in the application. A Notice of Appeal was timely filed on April 2, 2004, with the accompanying fee. Our check in the amount of $330.00 accompanies this Brief in accordance with 37 CFR §1.17(c).

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventors recorded in the files of the U.S. Patent and Trademark Office at Reel 9159, Frame 0921.

Related Appeals and Interferences

Applicant knows of no currently pending related appeals or interferences that would have an effect on the outcome of this appeal.

Status of Claims

Claims 9-12 and 14 are pending in this application and are before this Board for consideration on appeal. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

No amendments to the claims were filed after final rejection. All previous amendments have been entered.

Summary of the Invention

One embodiment of the present invention is directed to a semiconductor device or substrate which incorporates a layer of silicon dioxide which has been pretreated to provide a smooth morphology for a subsequently deposited layer of polycrystalline silicon. The pretreatment method includes implanting hydrogen ions into a layer of silicon dioxide by plasma source ion implantation and forming a layer of polycrystalline silicon on the layer of silicon dioxide such that the polycrystalline silicon layer is free of contaminants and has a smooth morphology.

In one embodiment of the invention illustrated in Fig. 1 and described at pages 7-10 of the specification, the layer 14 of silicon dioxide 16 comprises a layer in a semiconductor substrate 12. After the layer is doped by plasma source ion implantation, a layer 18 of polycrystalline silicon 20 is formed on the layer 14 of silicon dioxide.

In another embodiment illustrated in Fig. 2 and described at pages 10-11, the layer of silicon dioxide comprises a layer in a semiconductor substrate 52 which is part of a field effect transistor 50 comprising a gate oxide 54 and a source 56 and drain 58 formed on the semiconductor substrate. A layer of polysilicon 66 is formed on the gate oxide 54 to form a gate electrode 70. The surface of the substrate 52 is pretreated as described above so that the subsequently formed layer 64 of polysilicon 66 has a smooth morphology.

In another embodiment shown in Fig. 3 and described at page 12, the silicon dioxide layer may be formed on a semiconductor substrate which is part of a memory array 100 including a plurality of memory cells 102 which comprise at least one field effect transistor 50, a gate oxide for each of the field effect transistors, a source and drain for each of the field effect transistors, and a gate electrode for each of the field effect transistors.

In another embodiment illustrated in Fig. 4 and described at page 12, the layer of silicon dioxide is formed on a semiconductor substrate 52 which is incorporated in a semiconductor wafer W which comprises a repeating series of gate oxides, a repeating series of sources and drains, and a repeating series of gate electrodes.

In another embodiment illustrated in Fig. 5 and described at pages 13-14, a layer of silicon dioxide, glass or quartz comprising a semiconductor substrate 202 is doped with hydrogen ions as described above and then deposited with a layer of polycrystalline silicon 206. The semiconductor substrate is incorporated into a thin film transistor 200 which includes a gate oxide, a source and drain region formed in the polycrystalline silicon layer, and a gate electrode.

Issues Presented

The issues presented for review on appeal are:

1) Whether the Examiner erred in rejecting claim 9 under 35 U.S.C. 103(a) as being unpatentable over "applicant's admitted prior art" in view of Henley et al. (U.S. 6,083,324).

2) Whether the Examiner erred in rejecting claims 10-12 under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "applicant's admitted prior art" with Henley et al.

3) Whether the Examiner erred in rejecting claim 14 under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. 5,576,229) in view of "applicant's admitted prior art" and Henley et al.

4) Whether the Examiner has carried his burden of establishing a prima facie case of obviousness for any of the appealed claims 9-12 and 144.

Grouping of Claims

The Examiner has made three separate grounds of rejection, rejecting claim 9 under 35 U.S.C. 103(a) as being unpatentable over "applicant's admitted prior art" in view of Henley et al. (U.S. 6,083,324); rejecting claims 10-12 under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "applicant's admitted prior art" with Henley et al.; and rejecting claim 14 under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. 5,576,229) in view of "applicant's admitted prior art" and Henley et al. The application contains five rejected independent claims, namely, claims 9, 10, 11, 12, and 14. Applicant submits that the claims do not stand or fall together. The patentability of each independent claim will be separately argued.

The References

Applicant's admitted prior art. By "applicant's admitted prior art," the Examiner is referring to the discussion of the prior art Kaufman source implantation technique discussed at page 1, lines
12-22 of applicant's specification.

Henley et al. U.S. Patent No. 6,083,324. Henley et al. teach a method of providing a gettering layer in a silicon-on-insulator wafer using a plasma immersion ion implantation technique to implant ions, gas, or carbon as precipitate-forming particles beneath the surface of the silicon wafer, but above the surface of the insulating oxide layer. The precipitates act as gettering sites for impurities in the silicon layer of the wafer.

Burns et al., *Principles of Electronic Circuits*, pp. 380-381. Burns et al. teach a field effect transistor including a source and drain, a layer of silicon dioxide, and a gate electrode

formed of aluminum. Burns et al. also teach a read-only memory (ROM) structure including field effect transistors, source and drain regions, and polysilicon rows which act as a gate.

Murata et al., U.S. Patent No. 5,576,229. Murata et al. teach a method of forming a thin film transistor used in a liquid-crystal display apparatus. The thin film transistor is formed on a glass substrate and includes source and drain regions formed in a semiconductor thin film having a capping film (silicon oxide) thereon where hydrogen ions and metal ions are simultaneously implanted through the capping film and polysilicon film using a plasma source such that the resulting semiconductor thin film has low resistivity.

ARGUMENT

I. Summary of Argument

The Examiner has failed to establish a prima facie case, by evidence or reasoning, that any of the rejected claims would have been obvious with respect to the proposed combination of references. No motivation or suggestion exists to combine the teachings of "applicant's admitted prior art" with any of the cited references. The Examiner has used prohibited hindsight reconstruction in citing Henley et al. against the claims, requiring one skilled in the art to ignore the fact that Henley et al. do not teach or suggest providing a surface treatment on a silicon dioxide substrate for the purpose of providing a subsequent layer of polycrystalline silicon which has a smooth morphology as claimed.

II. The Examiner's burden of establishing a prima facie case of obviousness has not been met.

It is well established that the burden of establishing a prima facie case of obviousness resides with the Examiner. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Piasecki*, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). This burden can be satisfied only by showing some objective teaching in the prior art, or that knowledge generally available to one of ordinary skill in the art, would lead that individual to the claimed invention. Both the teaching

and a reasonable expectation of success must be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 20 USPQ2d 1438 (Fed.Cir. 1991).

Where the teachings of references are proposed to be combined, it is encumbent upon the Examiner to explain why the combination of reference teachings is proper. The suggestion to modify the reference teachings must come from the references themselves, not from applicant's disclosure. See *In re Laskowski*, 871 F.2d 115, 117, 10 USPQ2d 1397, 1398-99 (Fed. Cir. 1989); *In re Fine*, supra 837 F.2d at 1075 ("[T]eachings of references can be combined, only if there is some suggestion or incentive to do so. Here, the prior art contains none."); *Uniroyal v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 1051, 5 USPQ2d 1434 (Fed. Cir.), *cert. denied*, 109 S. Ct. 75 (1988) ("When prior art references require selective combination...to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself. Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination.") Applicant submits that the proposed combination of references here is not based on any objective teaching or suggestion in the references themselves, but rather is based on prohibited hindsight using the claimed invention as a blueprint. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985).

Applicants submit that upon close examination, the Examiner did not meet his burden of establishing a prima facie case of obviousness as to any of the claims on appeal.

III. "Applicant's admitted prior art" and Henley et al. are not properly combinable and do not provide any expectation of success.

With regard to the rejection of claim 9 based on "applicant's admitted prior art" and Henley et al., the Examiner maintained in the final rejection mailed March 3, 2004 that it would have been obvious to substitute a plasma source ion implantation (PSII) method as taught in Henley et al. for the Kaufman ion source method disclosed in "applicant's admitted prior art." While applicant pointed out that one would have to pick and choose hydrogen from among Henley's possible choices of ions, gases or carbon for use in the PSII technique, the Examiner

asserts that hydrogen implantation is taught by the admitted prior art and that Henley is only relied upon to teach that hydrogen may be implanted into semiconductor articles by a PSII method. However, this teaching alone does not provide proper motivation for the Examiner's proposed substitution. "Applicant's admitted prior art" and Henley et al. do not teach or suggest using the same methods to obtain the same desired result as the claimed invention. Henley et al. do not address the problem, and provide no expectation of a successful solution of that problem. Applicant's admitted prior art teaches pretreating the **surface** of a silicon dioxide layer with hydrogen ions to provide a smooth morphology for a subsequently deposited polysilicon layer. Henley et al. teach implanting various different ions, gases, or carbon **between** an insulating layer of silicon oxide and the top surface of the wafer. There is no motivation to combine the teachings as proposed by the Examiner as Henley et al. do not teach or suggest implanting hydrogen ions on the **surface** of a layer of silicon dioxide which is formed on a semiconductor substrate as claimed. While the Examiner asserts that he relied on applicant's admitted prior art for teaching a surface treatment, and that Henley et al. is "only" relied on for correcting the deficiencies of the prior art, i.e., metal contamination from the Kaufman ion source, the Examiner cannot choose to ignore the fact that Henley et al. do not teach a surface treatment, do not address the same problem, and provide no expectation of successful solution of that problem.

Nor do Henley et al. teach or suggest providing a layer of polycrystalline silicon formed on the doped layer of silicon dioxide which has a smooth morphology as claimed. While the Examiner has taken the position that this limitation is also taught by "applicant's admitted prior art," again, this teaching alone does not provide sufficient motivation to combine the teachings of the references. Further, the Examiner's assertion is factually incorrect because practice of the prior art Kaufman technique results in a metal-contaminated surface. One skilled in the art would not look to Henley et al. to correct the deficiencies of "applicant's admitted prior art" as Henley et al. teach implanting a variety of different materials **between** a layer of silicon dioxide and a wafer, not implanting hydrogen ions on the **surface** of a silicon dioxide layer for the purpose of providing a smooth morphology for the subsequently deposited polycrystalline silicon layer. As taught by applicant at page 10, lines 2-5, the implantation of hydrogen ions in the silicon dioxide substrate is believed to increase the number of nucleation sites for the subsequent

polycrystalline silicon deposition. Henley et al. do not teach or suggest the use of the PIII technique for this purpose.

Moreover, the fact that the references can be combined does not render the resultant combination obvious unless the prior art suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) and MPEP §2143.01. The desirability of the combination is clearly not suggested in the prior art. Rather, the Examiner's proposed combination of "applicant's admitted prior art" and Henley et al. is based on prohibited hindsight. The Examiner maintains at page 7 of the final office action that the motivation for combining the references lies in Henley et al.'s teaching that the PIII method produces less impurity metal contamination than other ion implantation techniques. However, Henley et al's technique is an ion **immersion** technique. There is nothing in Henley et al. which indicates that such a method would be applicable to the **surface** of a silicon dioxide layer and would successfully result in a layer of silicon dioxide which is free of metal contaminants as claimed. Nor do Henley et al. teach or suggest that the use of hydrogen plasma ions may be used to obtain a smooth morphology for a subsequently deposited polycrystalline silicon layer. It must also be remembered that Henley et al. suggest using a variety of ions, gases and carbon, and nothing in Henley et al. points specifically to the use of hydrogen ions. While the Examiner maintains that these limitations are "taught by the admitted prior art," (an assertion applicant has shown to be factually incorrect) there is nothing in Henley et al. which would provide motivation to one skilled in the art to use Henley's technique on the surface of a silicon dioxide layer to provide a smooth morphology for a subsequently deposited polycrystalline silicon layer.

The problem addressed and solved by the present invention is not addressed by Henley et al. Rather, Henley et al. are concerned with removing impurities from an SOI wafer by implanting particles **beneath** the wafer surface but **above** the insulating layer such that the particles form microbubbles or precipitates which act as gettering sites for the impurities in the silicon layer. Accordingly, one of ordinary skill in the art would not have looked to use the teachings of Henley et al. in conjunction with "applicant's admitted prior art" in order to resolve the problem the present invention addresses because Henley et al. deal with a completely different issue.

The reference teachings do not suggest any desirability or motivation to combine, nor do they provide any reasonable expectation of success. Claim 9 is clearly patentable because no prima facie case of obviousness has been established.

IV. The teachings of Burns et al., "Applicant's admitted prior art," and Henley et al. are not properly combinable and do not render claims 10-12 obvious.

The Examiner has admitted that Burns et al. do not teach a field effect transistor including a layer of silicon dioxide which includes hydrogen ions implanted therein or which is free of metal contaminants as recited in applicant's claim 10. The Examiner relies on the combined teachings of "applicant's admitted prior art" and Henley et al., reasoning that it would have been obvious to form the gate oxide of Burns et al. from a layer of silicon dioxide having hydrogen ions implanted therein such that the layer of polycrystalline silicon formed on the silicon dioxide would have a smooth morphology. As discussed extensively above, there is no suggestion in Henley et al. to implant hydrogen ions **on** a layer of silicon dioxide in a semiconductor substrate, nor any suggestion that such would provide a smooth morphology for a subsequently deposited layer of polycrystalline silicon. Nor is there any teaching or suggestion in Henley et al. of doing so on a silicon dioxide layer in a field effect transistor.

With regard to claim 11, which recites a memory array comprising a semiconductor substrate and a layer of silicon dioxide formed on the semiconductor substrate which has been pretreated by PSII, the Examiner refers to pages 380 and 381 of Burns et al. which disclose a read-only memory structure including a plurality of memory cells, asserting that it would have been obvious to form the gate oxide for each field effect transistor using a silicon dioxide layer having hydrogen ions implanted therein. Again, there is no teaching or suggestion in any of the references which would motivate one skilled in the art to combine their teachings to make the claimed memory array, nor do the cited references provide any expectation of success.

With regard to claim 12, the Examiner has taken the position that one of ordinary skill in the art would have formed the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die as claimed. However, the Examiner has failed

to cite any reference, alone or in combination, which teaches or suggests such a semiconductor wafer in which the layer of silicon dioxide formed on the semiconductor substrate has been implanted with hydrogen ions as claimed. Claim 10-12 are clearly patentable over the cited references because the Examiner has failed to establish a prima facie case of obviousness.

V. The teachings of Murata et al., "applicant's admitted prior art" and Henley et al. are not properly combinable and do not render claim 14 obvious.

Claim 14 recites a thin film transistor comprising a semiconductor substrate formed from silicon dioxide, quartz, or glass which has been implanted with hydrogen ions by a PSII method and which is free of metal contaminants. The Examiner admits at page 6 of the final rejection that Murata et al. do not teach a substrate which is free of metal contaminants as claimed. The Examiner has taken the position that it would have been obvious to implant hydrogen ions into the glass substrate of Murata et al. based on the teachings of "applicant's admitted prior art" and Henley et al. to achieve a substrate which is free of metal contaminants and in which a subsequently deposited polycrystalline silicon layer would have a smooth morphology. For the same reasons discussed extensively above, there is no motivation to combine the teachings of the references. There is no motivation to use the implantation process of Henley et al. on the **surface** of a semiconductor substrate as claimed, nor do any of the cited references indicate any expectation of success of obtaining a substrate which is free of metal contaminants and which provides a smooth morphology for a subsequently deposited polycrystalline silicon layer.

Further, Murata et al. do not address the problem solved by the claimed invention, but rather teach the implantation of hydrogen ions and metal ions into a semiconductor film for the purpose of obtaining a film having low resistivity. See col. 3, lines 27-37. Nothing in the prior art references provides motivation for preparing the glass surface of the substrate of Murata et al. such that it is free of metal contaminants and such that the subsequent deposition of a polycrystalline silicon layer has a smooth morphology as claimed because the Examiner has failed to establish a prima facie case of obviousness.

Claim 14 is clearly patentable over the cited combination of references.

VI. Conclusion

The prior art references clearly do not render obvious the claims on appeal as they do not teach or suggest a semiconductor device or related device which includes a layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation and a layer of polycrystalline silicon deposited on the layer of silicon dioxide which has a smooth morphology.

Conclusion

The Board is requested to reverse the rejections of claims 9-12 and 14 in their entirety.

Respectfully submitted,

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APPENDIX

The Claims on Appeal

9. A semiconductor device precursor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on said semiconductor substrate, said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of sputtered metal contaminants; and

a layer of polycrystalline silicon formed on said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology.

10. A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain formed in said semiconductor substrate with a gate electrode formed on said semiconductor substrate from said layer of polycrystalline silicon to form a field effect transistor.

11. A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor;

a gate oxide for each of said field effect transistors formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain for each of said field effect transistors formed in said semiconductor substrate; and

a gate electrode for each of said field effect transistors formed on said semiconductor substrate from said layer of polycrystalline silicon.

12. A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a repeating series of gate oxides formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a repeating series of sources and drains for at least one field effect transistor formed on each of said plurality of die, said series of sources and drains being formed on said semiconductor substrate; and

a repeating series of gate electrodes for at least one field effect transistor formed on each of said plurality of die, said series of gate electrodes being formed on said semiconductor substrate from said layer of polycrystalline silicon.

14. A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of said semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of an insulating material formed on at least a portion of said layer of polycrystalline silicon;

a gate oxide formed from said layer of insulating material;

a source region and a drain region formed in said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.